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eFiled Application Information

EFS ID	5071964
Application Number	10072506
Confirmation Number	2876
Title	SORT PROCESSING METHOD AND SORT PROCESSING APPARATUS
First Named Inventor	Masatoshi Imai
Customer Number or Correspondence Address	24201
Filed By	Howard Sommers/Valerie D'Angelo
Attorney Docket Number	59227/SONYP
Filing Date	05-FEB-2002
Receipt Date	31-MAR-2009
Application Type	Utility under 35 USC 111(a)

Application Details

Submitted Files	Page Count	Document Description	File Size	Warnings
STATUS_SONYP-59227.pdf	1	Miscellaneous Incoming Letter	48674 bytes	PASS
REQUEST_FOR_CERTIFICATE_OF_CORRECTION_SONYP-59227.PDF	8	Miscellaneous Incoming Letter	209505 bytes	PASS
CERTIFICATE_OF_CORRECTION_SONYP-59227.PDF	1	Miscellaneous Incoming Letter	38343 bytes	PASS

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New International Application Filed with the USPTO as a Receiving Office

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ELECTRONIC TRANSMISSION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No.	:	7,370,046 B2	Confirmation No. :	2876
Inventor	:	Masatoshi Imai		
Issued	:	May 6, 2008		
Art Unit	:	2161		
Examiner	:	Cam Linh T. Nguyen		
Title	:	SORT PROCESSING METHOD AND SORT PROCESSING APPARATUS		
Docket No.:	:	SONYP 59227		
Customer No.	:	24201		

STATUS REQUEST REGARDING
REQUEST FOR CERTIFICATE OF CORRECTION

Dear Sir:

Please advise regarding the status of the attached Request for Certificate of Correction for the above patent.

Respectfully submitted,

FULWIDER PATTON LLP

Date: March 31, 2009

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Customer No. 24201

ELECTRONIC FILING

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No.	:	7,370,046 B2	Confirmation No. :	2876
Inventor	:	Masatoshi Imai		
Issued	:	May 6, 2008		
Art Unit	:	2161		
Examiner	:	Cam Linh T. Nguyen		
Title	:	SORT PROCESSING METHOD AND SORT PROCESSING APPARATUS		
Docket No.:	:	SONYP 59227		
Customer No.	:	24201		August 6, 2008

REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The above-identified patent has been found to have the errors set forth in the enclosed Certificate of Correction. It is requested that this Certificate of Correction be issued and returned to us. Since the errors occurred in the final printing phase of the patent, no fee is enclosed. However, should the Office determine that a fee is required, please charge Deposit Account No. 06-2425.

The errors are verifiable in the patent application file as follows:

ERRORS	APPLICATION FILE
Column 2, line 16, start new paragraph with "A converter **5**".	Specification dated February 5, 2002, page 4. See attachment.
Column 11, line 59, after "respectively" insert --.-- (a period).	Specification dated February 5, 2002, page 33. See attachment.
Column 11, line 59, start new paragraph with "By the same token".	Specification dated February 5, 2002, page 33. See attachment.
Column 12, line 30, delete "Dil" and insert --Di**1**--.	Specification dated February 5, 2002, page 35. See attachment.
Column 12, line 32, delete "on" and insert --On--.	Specification dated February 5, 2002, page 35. See attachment.
Column 14, line 6, delete "FBG" and insert --FB**6**--.	Specification dated February 5, 2002, page 40. See attachment.
Column 17, line 53, delete ".o" and insert --.-- (period).	Specification dated February 5, 2002, page 50. See attachment.
Column 17, line 53, start new paragraph with "By adopting".	Specification dated February 5, 2002, page 50. See attachment.

These errors occurred in good faith and correction thereof does not involve such changes in the patent as would constitute new matter or would require re-examination.

It is requested that a Certificate of Correction be issued and returned to us.

Attached hereto is Form PTO/SB/44 which is suitable for printing.

Respectfully submitted,

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By: /howard n. sommers/ HNS
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299254.1

(2) with pieces of input data received by the input terminals Y1-(0) to Y1-(7). Likewise, the comparators 2-(70) to 2-(76) compare the input data received by the input terminal X1-(7) with pieces of input data received by the input terminals Y1-(0) to Y1-(7).

An adder 3-(0) sums up comparison results of seven bits output by the comparators 2-(01) to 2-(07). By the same token, an adder 3-(1) sums up comparison results of seven bits output by the comparator 2-(10) and the comparators 2-(12) to 2-(17). In the same way, adder 3-(2) sums up comparison results of seven bits output by the comparators 2-(20) to 2-(27). Likewise, an adder 3-(7) sums up comparison results of seven bits output by the comparators 2-(70) to 2-(76).

A converter 5 converts the priority levels D40 to D47 output by the adders 3-(0) to 3-(7) respectively into 3-bit priority signals D60 to D67 respectively. The 3-bit priority signals D60 to D67 each indicate which piece of input data is largest.

Multiplexers 7-(0) to 7-(7) each receive eight pieces of data through input terminals Z1-(0) to Z1-(7). These eight pieces of input data are the same pieces of input data supplied to the input terminals X1-(0) to X1-(7) and Y1-(0) to Y1-(7). That is to say, input data

K17(0) to the output terminal Ko1 and the key data K17(1) to the output terminal Ko2. If the basic cell 18-(0) supplies the key data K17(0) to the output terminal Ko1 and the key data K17(1) to the output terminal Ko2, the relevant data D17(0) and the relevant data D17(1) are supplied to the output terminals Do1 and Do2 respectively. If the basic cell 18-(0) supplies the key data K17(0) to the output terminal Ko2 and the key data K17(1) to the output terminal Ko1, the relevant data D17(0) and the relevant data D17(1) are supplied to the output terminals Do2 and Do1 respectively.

By the same token, a compound-data pair C17(2) of relevant data D17(2) and key data K17(2) are supplied to respectively external input terminals 17-(20) and 17-(21) of a first-stage basic cell 18-(1), whereas another compound-data pair C17(3) of relevant data D17(3) and key data K17(3) are supplied to respectively external input terminals 17-(30) and 17-(31) of the first-stage basic cell 18-(1). In the same way, a compound-data pair C17(4) of relevant data D17(4) and key data K17(4) are supplied to respectively external input terminals 17-(40) and 17-(41) of a first-stage basic cell 18-(2), whereas another compound-data pair C17(5) of relevant data D17(5) and key data K17(5) are supplied to respectively external input

data K17(7) to the output terminal Ko1, on the other hand, the relevant data D17(6) and the relevant data D17(7) are supplied to the output terminals Do2 and Do1 respectively.

Input terminals Di1 and Ki1 of a second-stage basic cell 18-(4) are connected to respectively the output terminals Do2 and Ko2 of the first-stage basic cell 18-(0). On the other hand, input terminals Di2 and Ki2 of the second-stage basic cell 18-(4) are connected to respectively the output terminals Do1 and Ko1 of the first-stage basic cell 18-(1).

In the same way, input terminals Di1 and Ki1 of a second-stage basic cell 18-(5) are connected to respectively the output terminals Do2 and Ko2 of the first-stage basic cell 18-(1). On the other hand, input terminals Di2 and Ki2 of the second-stage basic cell 18-(5) are connected to respectively the output terminals Do1 and Ko1 of the first-stage basic cell 18-(2).

By the same token, input terminals Di1 and Ki1 of a second-stage basic cell 18-(6) are connected to respectively the output terminals Do2 and Ko2 of the first-stage basic cell 18-(2). On the other hand, input terminals Di2 and Ki2 of the second-stage basic cell 18-(6) are connected to respectively the output terminals Do1 and Ko1 of the first-stage basic cell 18-(3).

basic block FB5 outputs the eight sorted pieces of data as pairs of compound data to the basic block FB6.

The two inputs of compound data output by the basic block FB7 are supplied to seventh-stage basic cells 18-(21) to 18-(24) of a next basic block FB8, which also includes eighth-stage basic cells 18-(25) to 18-(27) in the same way as the pieces of compound data D9(0) to D0(7) are supplied to the first-stage basic cells 18-(0) to 18-(3) of the basic block FB5.

In the same way as the first-stage basic cells 18-(0) to 18-(3) are connected to the second-stage basic cells 18-(4) to 18-(6) in the basic block FB5, the seventh-stage basic cells 18-(21) to 18-(24) are connected in series to the eighth-stage basic cells 18-(25) to 18-(27) to form a similar pipeline configuration in the basic block FB8. In the basic block FB8, pieces of data, which are sorted by the seventh-stage basic cells 18-(21) to 18-(24), are supplied to the three eighth-stage basic cells 18-(25) to 18-(27). As a result, the basic block FB8 outputs eight sorted pieces of compound data as final pairs of output data to pairs of external output terminals 19-(00) and 19-(71) respectively in the same way as the basic block FB5 outputs the eight sorted pieces of data as pairs of compound data to the basic

increased to N/2. The pair of input terminals Ai and Bi of the basic cell 23-(0) to 23-(N/2-1) are connected to external input terminals 22-(0) and 22-(N-2) respectively.

Then, much like the second stage shown in Fig. 1, a second stage for the sort processing apparatus shown in Fig. 6 is sandwiched by a line connected to an output terminal Ao of the basic cell 23-(0) and a line connected to an output terminal Bo of the basic cell 23-(N/2-1). This second stage comprises (N/2-1) basic cells 24-(0) to 24(N/2-2). Input terminals Ai and Bi of the second-stage basic cell 24-(1) to 24-(N/2-2) are connected to respectively an output terminal Bo of the first-stage basic cell 23-(0) to 23-(N/2-1) and an input terminal Ao of the first-stage basic cell 23-(0) to 23-(N/2-1). The N/2 first-stage input basic cells 23-(0) to 23-(N/2-1) and the second-stage basic cells 24-(0) to 24-(N/2-2) form a first basic block 25-(0).

This extended sort processing apparatus comprises N/2 basic blocks 25-(0) to 25-(N/2-1), which are arranged in the horizontal direction. The last basic block 25-(N/2-1) has external output terminals 26-(0) to 26-(N/2-1).

By adopting the extension technique described above, an increased number of pieces of input data can be